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A SOLUTION OF THE POWER SYSTEM LOAD FLOW PROBLEM ON THE DIGITAL COMPUTER USING THE IMPROVED D C LOAD FLOW TECHNIQUE

by

Dr. J. Rohan Lucas, Dr. Abhaya S. Induruwa and Alexander S. Malembeka

Abstract

This paper presents an improved d.c. load flow (IDCLF) technique for obtaining the a.c. load flow solution of a power system on the digital computer. The computer program developed is based on a similar technique on the d.c. network analyser by Karunaratne et al.

The technique on the computer was developed as the Network Analyser solution was extremely slow and cannot be used for comparison studies, where fast solutions are of paramount importance. Also, previously developed a.c. load flow solutions were too time consuming and d.c. load flow techniques on the computer did not give a complete a.c. load flow solution.

The technique has been tested against the proven Fast Decoupled Load Flow (FDLF) solution and shown to give reasonable results for the IEEE 14 bus test system.

Although, in the present study, saving in storage or computer time was not significant, this is due to the fact that the advantages of sparsity has not been exploited in the program.

List of Symbols

Bik	-	susceptance of line ik
[H]	-	top diagonal sub-matrix of Jacobian
Ii, Ik	-	currents at ends i and k
[L]	-	bottom diagonal sub-matrix of Jacobian
Pik	-	active power flow of line iK
q	-	charge flow in line
Qik	-	reactive power flow of iK
Qik^m	-	modified Qik
rik	-	resistance of line iK
Si	-	complex power, node i
Vi, Vk	-	voltages at ends i and k
vik	-	voltage across line ik
xik	-	reactance of line iK
Xik	-	equivalent Xik
Yik^{sh}	-	shunt admittance, iK
θ i, θk	-	voltage angles at ends i & K
θ ik	-	voltage angle across line iK
θ ik'	-	modified θiK

1.0 Introduction

In load flow studies where the speed of calculation is a priority, solution by d.c. load flow is generally more efficient than the corresponding a.c. load flow solution. However, in the past, it found limited use in various studies of power systems

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because of its inability to provide estimates of bus voltage magnitudes. It provided estimates of power flows only[1]. The problem has been solved[2,3] on the d.c. network analyser, by presenting a d.c. load flow technique capable of simulating both the active and the reactive power in successive simulations. However, these techniques were not directly solvable on the digital computer.

The technique on the computer was developed as the Network analyser solution is tedious, the size of the system that can be studied is limited, and a special purpose analog computer is otherwise required. A computer technique, which is both fast and sufficiently accurate is required for comparison studies, especially in reliability studies. This computer technique has been developed especially with this in mind.

In the present paper, the application of the d.c. network analyser technique has been extended to the digital computer by suitable modifications. The computer program developed has been tested by application to the 14-bus IEEE test power system[4].

2.0 The Load Flow Problem on the D.C. Network Analyser

The use of the d.c. network analyser for the study of the a.c. load flow problem was first formulated by Karunaratne[2] by making certain basic assumptions. These are

i. all voltage angles at the busbars are small
ii. transformers are on nominal tap
iii. all voltages are 1.0 p.u.
iv. all shunt elements have negligible value
v. all line resistances have negligible value.

However, the reactive losses in the lines are not wholly neglected, but accounted for by modifying the reactive power injections at the respective nodes.

With this method, an appreciable error (of more than 15%) arose when the technique was used to solve the load flow problem of power systems with transmission lines having low x/r ratios, so that only systems with lines having a high x/r ratio could be studied. The method was subsequently improved by Karunaratne et al[3] by including the line resistance and the shunt capacitance of each line. In this improvement, what is initially obtained is the modified bus voltage angle and the active power flows. A modified reactive power (taking into account the contributions caused by reactive power loss, reactive power generation by shunt capacitors and the reactive power flow due to angle difference) is used to calculate the voltage magnitude of the busbars and the modified reactive power flow in the lines. The actual bus voltage angles and the actual reactive power flows are finally determined by suitable corrections. With these improvements, the technique is capable of solving load flow problems even for power systems whose transmission lines have a low x/r ratio.

2.1 D. C. Load Flow Technique for low x/r ratios

The inclusion of the resistance of the lines, the shunt admittance of the lines and the accompanying modifications, add the following advantages.

(see Appendix A1 for details)

i. It is possible to correct the bus voltage angles from those obtained initially, using

$$Oik = \frac{Oi' - Ok'}{Vi\ Vk} - \frac{rik}{Xik}\ (Vi - Vk)$$

ii. It is possible to consider the contribution to reactive power flow caused by the difference in voltage across a line, by the term

$$P_{ik}.(r_{ik}/X_{ik})$$

iii. The reactive power generated by the line capacitances can be considered, by the term $y_{ik}^{sh/2}$.

3.0 Modification of the D.C. Load Flow Network Analyser Technique for use on a Digital Computer

The Network analyser solution is obtained by the successive balancing of the injected power flows cyclically, till erros become within limits. On the computer, the cyclical balancing is not carried out, but instead the solution is obtained in one go by solving the corresponding set of equations.

A step by step description of the technique on the computer, is shown in the flow diagram of figure 3.1 and the salient points are described in the following section.

3.1 Calculation of Modified Bus Voltage Angles θ

The modified bus voltages angles θ are calculated by using equation A1.8 corresponding to the operation in the Network Analyser.

$$[P] = [H]\,[\theta']$$

3.2 Calculation of the Modified Bus Reactive Power Q^m

The modified reactive power Q^m is required in order to calculate the voltage magnitudes using equation A1.9. However, the modified reactive power should first be calculated using equation A1.7. In this equation, the active power flow Pik is not yet known. In the d.c. network analyser, the active power flow is measured

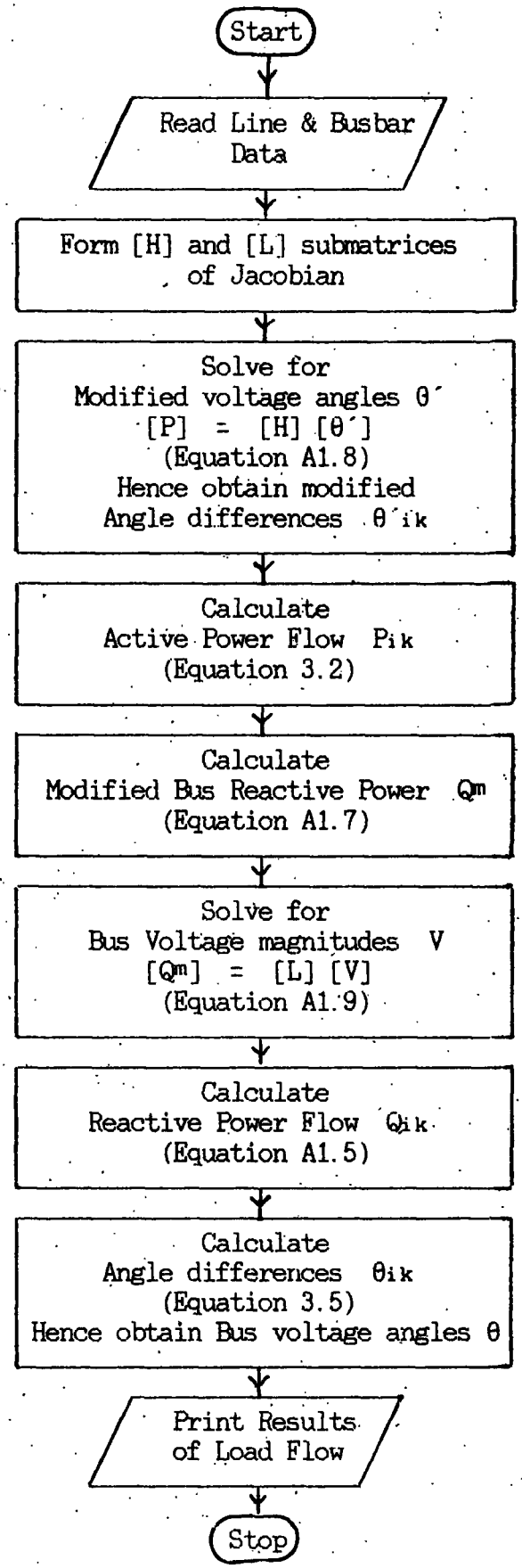

Figure 3.1 Flow Diagram of IDCLF

after simulation of the active power injection, but in the case of a digital computer, it must be calculated using the expression for active power flow, given by equation 3.1.

$$P_{ik} = (r_{ik} V_i^2 - r_{ik} V_i V_k \cos\theta_{ik}' + X_{ik} V_i V_k \sin\theta_{ik}') / (X_{ik}^2 + r_{ik}^2) \quad \ldots\ldots (3.1)$$

The only unknown quantities in calculating Pik are voltages Vi and Vk. If these voltages are assumed 1.0 p.u., equation 3.1 reduces to

$$P_{ik} = (r_{ik} - r_{ik} \cos\theta_{ik}' + X_{ik} \sin\theta_{ik}') / (X_{ik}^2 + r_{ik}^2) \quad \ldots\ldots (3.2)$$

Equation 3.2 is used to calculate the active power flow which is needed in equation A1.7. (This equation 3.2 gives more accurate results than when equation A1.4 is used).

The admittance matrix in the calculations is formed by using the line susceptances

$$B_{ik} = X_{ik}/(X_{ik}^2 + r_{ik}^2)$$

and not the inverse of the line series reactance.

3.3 Calculation of Power Flows

The active and reactive power flows are calculated by using equation A1.4 and A1.6, which are reproduced below.

$$P_{ik} = \theta_{ik}'/\hat{X}_{ik}$$

$$Q_{ik}^m = V_{ik}/X_{ik}$$

where $\hat{X}_{ik} = (X_{ik}^2 + r_{ik}^2) / X_{ik}$

However, the modified reactive power flow Q_{ik}^m is not yet known. In the d.c. network analyser, Q_{ik}^m is measured after simulation of reactive power, but in the case of the digital computer, the Qik must be calculated. The exact expression for the reactive power flow is given by equation 3.3.

$$Q_{ik}^m = (X_{ik} V_i^2 - X_{ik} V_i V_k \cos\theta_{ik} - r_{ik} V_i V_k \sin\theta_{ik}) / (X_{ik}^2 + r_{ik}^2) \quad \ldots\ldots (3.3)$$

Making the assumptions cos θik = 1 and rik = 0, equation 3.3 reduces to

$$Q_{ik}^m = V_i (V_i - V_k) / X_{ij} \quad \ldots (3.4)$$

Equation (3.4) is used to calculate the approximate reactive power flow Q_{ik}^m required.

3.4 Calculation of the Effective Bus Voltage Angles θ

As pointed out earlier, equation A1.7 is used to calculate the modified bus angles θ. With the voltage magnitudes and the modified angles known, the effective bus angles θ are obtained by correcting the effective voltage angle differences across a line using equation 3.5.

$$\theta_{ik} = \theta_{ik}'/(V_i V_k) \quad (r_{ik}/X_{ik})(V_i - V_k) \quad \ldots\ldots (3.5)$$

4.0 Application of the Technique and Results

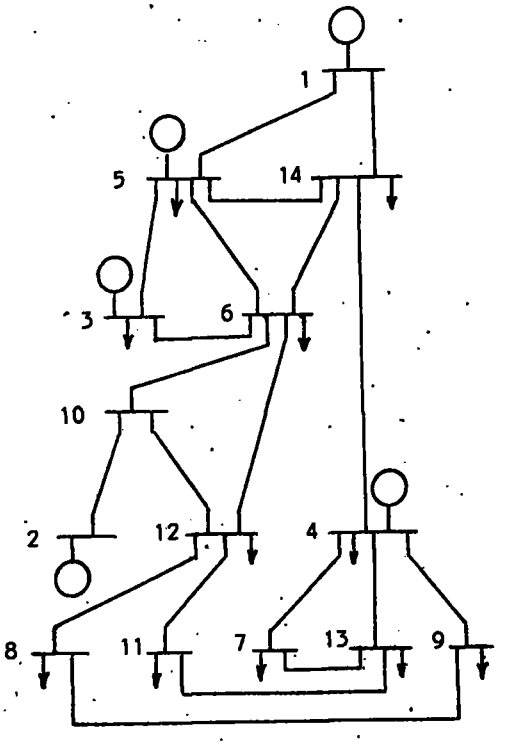

Figure 4.1 - IEEE 14 Bus test system

The technique was tested by applying it to the IEEE 14 Bus Test Power System[4]. The FDLF technique[5] was applied to the same system in order to compare the accuracy of the technique developed.

The line diagram for the system is shown in figure (4.1). A comparison of the loadings are shown in table (4.1). The corresponsing power flows are shown in table (4.2).

The storage requirement of the Improved DC Load Flow Technique including its Subroutines is 6.048 K, and the CPU time required for loading and executing the Improved DC Load Flow Technique is 14.569s on an IBM 1130 Computer.

5.0 Conclusions

The improved d.c. load flow technique has been implemented on the digital computer. The results of the Load flow analysis for the 14 bus IEEE test system show that the accuracy of the Improved DC Load Flow Technique is reasonable in comparison with the proven FDLF technique. However, it is found that the method is not advantageous when high accuracy is desired.

The Improved DC Load Flow technique can be used particularly in studies requiring fast solutions where high accuracy may not be necessary. Security monitoring is a typical example of such studies.

Economy in computation time and storage requirements can be achieved if sparsity programming is employed because only non-zero elements of the bus admittance matrix are stored and operated on.

6.0 References

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7.0 Acknowledgement

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APPENDIX A1 - D C Load Flow Technique for Low x/r ratios

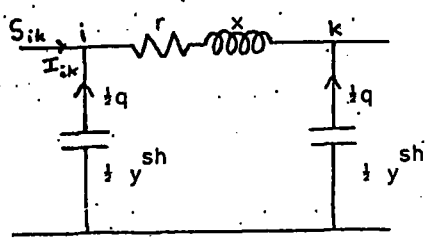

Figure A1.1 Equivalent Circuit for Line

The complex power flowing in line ik of figure A1.1, at node i is expressed as

$$S_{ik} = P_{ik} - j\,Q_{ik} = V_i^* . I_{ik} \quad \text{----(A1.1)}$$

$$= V_i^* . (V_i - V_k)/(r+jx) + j\,q/2$$

$$= j\,V_i . y_{ik}^{sh}/2 + [V_i (V_i - V_k \cos\theta_{ik}) + j\,V_i\,V_k \sin\theta_{ik}]/(r+jx) \quad \text{----(A1.2)}$$

In practice all the voltage angles θ are generally small so that

$$\sin\theta_{ik} = \theta_{ik} \text{ and } \cos\theta_{ik} = 1 - \theta_{ik}^2/2$$

Introducing these approximations in equation A1.2 we get

$$P_{ik} - j\,Q_{ik} = V_i (V_{ik} + V_k . \theta_{ik}^2/2 + j\,V_k\theta_{ik}) * (r - jx) + j y_{ik}^{sh}/2 \quad \text{----(A1.3)}$$

where $V_{ik} = V_i - V_k$

A1.1 Active Power Flow

Considering the real parts and neglecting the second order terms gives

$$P_{ik} = (V_i\,V_k/x_{ik})(\theta_{ik} - (r_{ik}/x_{ik}) * V_{ik})$$

$$= \theta_{ik}'/\hat{x}_{ik} \quad \text{----(A1.4)}$$

where $\theta_{ik}' = \theta_{ik} + (r_{ik}/x_{ik}) * V_{ik}$

$$\hat{x}_{ik} = (x_{ik}^2 + r_{ik}^2)/x_{ik}$$

A1.2 Reactive Power Flow

Considering the imaginary parts of equation A1.3 and assuming voltages V_i and V_k to be unity, gives

$$Q_{ik} = (V_{ik} + \theta_{ik}^2/2 - (r_{ik}/x_{ik}).\theta_{ik} - y_{ik}^{sh}/2)/\hat{x}_{ik} \quad \text{-----(A1.5)}$$

substituting for θ_{ik} and rearranging the terms gives

$$Q_{ik} - P_{ik}\,\theta_{ik}'/2 - (r_{ik}/x_{ik})\,V_{ik}^2/2 + (r_{ik}/x_{ik}).P_{ik}(1.+V_{ik}) + y_{ik}^{sh}/2 = V_{ik}/x_{ik}$$

i.e. $Q_{ik}^m = V_{ik}/x_{ik}$ -----(A1.6)

where

$$Q_i^m = Q_i + \sum_{k \in i} (-P_{ik}\,\theta_{ik}'/2 + (r_{ik}/x_{ik})P_{ik} + y_{ik}^{sh}/2) \quad \text{-----(A1.7)}$$

In matrix form, equations A1.4 and A1.6 can be written as

$$[P] = [H]\,[\theta'] \quad \text{-----(A1.8)}$$

$$[Q^m] = [L']\,[V] \quad \text{-----(A1.9)}$$

In the d c network analyser implementation of the a c load flow, the values of power flow in the individual lines of the network are based on equations A1.4 and A1.6. However, in the improved dc load flow technique on the computer, the corresponding expressions are obtained direct from the exact expression A1.2, with only the voltage magnitudes being approximated to 1.0 pu. This gives an overall improvement in the accuracy without sacrificing time.

BUS NO.	VOLTAGE (PU) FDLF	IDCLF	ANGLE (DEGREE) FDLF	IDCLF	ACTIVE POWER FDLF	IDCLF	REACTIVE POWER FDLF	IDCLF
1	1.0600	1.0600	0.00	0.00	2.327	2.222	-0.195	-0.186
2	1.0900	1.0900	-14.15	-13.99	0.000	0.000	0.309	0.359
3	1.0108	1.0108	-12.67	-12.34	-0.942	-0.942	0.024	0.021
4	1.0700	1.0700	-14.45	-13.74	-0.112	-0.112	0.529	0.548
5	1.0450	1.0450	- 4.97	- 4.68	0.183	0.183	0.235	0.246
6	1.0252	1.0380	-10.41	-10.12	-0.478	-0.478	0.039	0.039
7	1.0342	1.0228	-14.55	-13.61	-0.061	-0.061	-0.160	-0.160
8	1.0361	1.0276	-14.65	-14.56	-0.090	-0.090	-0.058	-0.058
9	1.0494	1.0400	-14.67	-14.71	-0.035	-0.035	-0.018	-0.018
10	1.0401	1.0319	-14.15	-13.99	0.000	0.000	0.000	0.000
11	1.0208	1.0114	-15.74	-15.72	-0.149	-0.149	-0.050	-0.050
12	1.0378	1.0300	-14.35	-14.21	-0.295	-0.295	-0.166	-0.166
13	1.0408	1.0304	-15.19	-14.33	-0.135	-0.135	-0.058	-0.058
14	1.0319	1.0413	- 8.92	- 8.59	-0.076	-0.076	-0.016	-0.016

Table 4.1 - Bus Loadings for IEEE 14 Bus Test Power System

LINE NO	SB	EB	REACTIVE POWER FDLF	IDCLF	ACTIVE POWER FDLF	IDCLF
1	1	5	-0.17	-0.16	1.56	1.49
	5	1	0.30	0.26	-1.52	-1.44
2	1	14	-0.01	-0.04	0.76	0.74
	14	1	0.11	0.13	-0.73	-0.71
3	6	10	-0.06	0.04	0.33	0.35
	10	6	0.08	-0.02	-0.33	-0.35
4	3	5	0.04	0.03	-0.71	-0.70
	5	3	0.06	0.06	0.73	0.73
5	3	6	-0.01	0.08	-0.24	-0.22
	6	3	0.00	0.08	0.24	0.23

LINE NO	SB	EB	REACTIVE POWER FDLF	REACTIVE POWER IDCLF	ACTIVE POWER FDLF	ACTIVE POWER IDCLF
6	4	7	0.12	0.16	0.06	0.07
	7	4	-0.11	-0.15	-0.06	-0.07
7	4	9	0.08	0.14	0.06	0.05
	9	4	-0.08	-0.13	-0.06	-0.05
8	4	13	0.15	0.24	0.19	0.16
	13	4	-0.14	-0.23	-0.18	-0.16
9	4	14	0.18	0.14	-0.42	-0.39
	14	4	-0.14	-0.10	0.42	0.39
10	5	6	-0.04	-0.12	0.56	0.55
	6	5	0.09	0.15	-0.55	-0.53
11	5	14	-0.04	-0.10	0.41	0.40
	14	5	0.07	0.11	-0.40	-0.39
12	10	2	-0.29	-0.34	0.00	0.00
	2	10	0.31	0.36	0.00	0.00
13	6	12	-0.02	0.02	0.13	0.14
	12	6	0.03	-0.01	-0.13	-0.14
14	6	14	0.05	0.13	-0.64	-0.64
	14	6	0.03	0.12	0.64	0.65
15	7	13	-0.05	-0.05	0.01	0.01
	13	7	0.05	0.05	-0.01	-0.01
16	8	9	-0.06	-0.06	-0.02	-0.01
	9	8	0.06	0.06	0.02	0.01
17	12	8	0.00	0.01	-0.07	-0.08
	8	12	-0.00	-0.00	0.07	0.08
18	10	12	0.21	0.18	0.33	0.35
	12	10	-0.21	-0.18	-0.33	-0.35
19	11	12	-0.01	-0.02	-0.10	-0.11
	12	11	0.02	0.02	0.10	0.11
20	11	13	-0.04	-0.04	-0.05	-0.04
	13	11	0.04	0.04	0.05	0.04

Table 4.2 - Power Flow for IEEE 14 Bus Test Power System